

REMARKS

Claims 1-31 are pending in the application. Claims 1, 8, 19, and 29 have been amended as indicated below. It is respectfully submitted that no new matter has been added.

Original Claim Rejections under 35 U.S.C. § 103

Claims 1-31 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Scott et al., U.S. Patent No. 5,870,046 (hereinafter "Scott") in view of Staffiere, U.S. Patent No. 6,137,671 (hereinafter "Staffiere").

Applicants filed on April 16, 2004 a declaration of inventors Beutler and Rahamim to establish that the present invention predates the filing date of Staffiere. Examiner states that "the evidence submitted is insufficient to establish applicant's alleged actual reduction to practice of the invention in this country or a NAFTA or WTO member country after the effective date of the Staffiere reference." Applicant respectfully submits that Examiner has misinterpreted the requirements of 37 CFR 1.131. No requirement exists requiring Applicants to establish Applicants' *actual* reduction to practice. See MPEP §715. Applicants respectfully submit that they have established by declaration the completion of the invention in the United States at a date prior to January 29, 1998, which is the effective date of Staffiere.

Applicant respectfully submits, therefore, that Staffiere does not qualify as prior art for purposes of 35 U.S.C. § 103(a).

Additional Claim Rejections under 35 U.S.C. § 103

Claims 1-31 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Scott et al., U.S. Patent No. 5,870,046 (hereinafter "Scott") in view of Ozawa et al., U.S. Patent No. 5,172,304 (hereinafter "Ozawa").

According to an embodiment of the present invention, the line side circuitry and the system side circuitry are both located on the same side of the substrate, and a conductive via through the substrate is utilized to connect the electrode on the far side of the substrate to the

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circuitry. See, for example, page 11, lines 7-14; page 11, line 25 – page 12, line 2; and Figures 2A, 2B, 3A, and 3B. Claims 1, 8, 19, and 29 have been rewritten to further bring out this feature of the present invention. No new matter has been added.

As per claims 1, 8, 19, and 29, Applicant respectfully submits that neither Scott, Ozawa, nor any combination thereof teaches or suggests a high voltage isolation barrier structure, comprising: a circuit board comprising a substrate, the substrate comprising a first side and a second side, the *first side having a first circuitry and a second circuitry*; a capacitive structure comprising: a first electrode disposed on the first side of the substrate; and a second electrode disposed on the second side of the substrate; and *a conductive via through the substrate*; and wherein the substrate intermediate the first and second electrodes functions as a dielectric material within the capacitive structure; the first electrode is electrically coupled to said first circuitry; and the *conductive via electrically couples the second electrode to the second circuitry*.
(As Amended)

Ozawa generally discloses a flat capacitor-containing wiring board, and Scott generally discloses an isolation system using discrete capacitors. Neither Ozawa, Scott, nor any combination thereof teaches using a conductive via to route an electrical path from one side of the substrate to the other in order that both circuitry are located on the same side of the substrate.

Applicant respectfully submits, therefore that claims 2-7, 9-18, 20-28, and 30-31 are allowable as depending from allowable base claims.

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CONCLUSION


For all the above reasons, the Applicant respectfully submits that this application is in condition for allowance. A Notice of Allowance is earnestly solicited.

The Examiner is invited to contact the undersigned at (214) 939-4618 to discuss any matter concerning this application. The Office is hereby authorized to charge any additional fees or credit any overpayments under 37 C.F.R. § 1.16 or § 1.17 to Deposit Account No. 50-0530.

Respectfully submitted,
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By: _____


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